Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled).

2. (Currently Amended) The method of claim 7~~1~~, wherein initiating a platform-independent device removal sequence for said ~~device~~ processor in response to detecting said event associated with said processor ~~device~~ comprises generating a system control interrupt.

3. (Original) The method of claim 2, wherein generating a system control interrupt comprises generating a system control interrupt utilizing an INT_OUT command.

4. (Cancelled).

5. (Currently Amended) The method of claim 74, wherein detecting an event associated with ~~a device~~ said processor within a data processing system comprises detecting an error within at least one of said first processor core and said second processor core.

6. (Currently Amended) The method of claim 74, said method further comprising disabling interrupts to said processor in response to initiating said~~a~~ platform-independent device removal sequence ~~for said device~~.

7. (Currently Amended) A ~~The~~ method ~~of claim 4, wherein~~ comprising:

operating a processor including a ~~said~~ first processor core and ~~said~~ a second processor core in a functional redundancy check mode comprises concurrently executing a thread on said first processor core and said second processor core~~, said method further comprising:~~;

detecting an event associated with said processor within a data processing system;

initiating a platform-independent device removal sequence for said processor in response to detecting said event associated with said processor;

saving a context of said thread in response to initiating said~~a~~ platform-independent device removal sequence~~ for said device~~;

virtually ejecting said processor from said data processing system in response to initiating said platform-independent device removal sequence for said device; and

servicing said event associated with said processor in response to virtually ejecting said processor from said data processing system.

8. (Original) The method of claim 5, said method further comprising disabling said functional redundancy check mode in response to detecting said error within at least one of said first processor core and said second processor core.

9. (Currently Amended) The method of claim 8, wherein servicing said event associated with said processor ~~device~~ in response to virtually ejecting said processor ~~device~~ from said data processing system comprises:

resetting said processor; and

re-enabling said functional redundancy check mode in response to resetting said processor.

10. (Currently Amended) The method of claim 7~~1~~, said method further comprising:

initiating a platform-independent device insertion sequence for said processor ~~device~~ in response to servicing said event associated with said processor~~device~~; and

virtually inserting said processor ~~device~~ into said data processing system in response to initiating said platform-independent device insertion sequence for said processor~~device~~.

11. (Cancelled).

12. (Cancelled).

13. (Currently Amended) The machine-accessible medium of claim ~~12~~15, wherein detecting an event associated with said processor ~~a device~~ within said~~a~~ data processing system

comprises detecting an error within at least one of said first processor core and said second processor core.

14. (Currently Amended) The machine-accessible medium of claim ~~12~~15, said method further comprising disabling interrupts to said processor in response to initiating said~~a~~ platform-independent device removal sequence~~ for said device~~.

15. (Currently Amended) A The machine-accessible medium ~~of claim 12, wherein~~ having machine-executable instructions embodied therein which, when executed by a machine, causes said machine to perform a method comprising:

operating a processor including ~~said~~ a first processor core and ~~said~~ a second processor core in a functional redundancy check mode ~~comprises~~ by concurrently executing a thread on said first processor core and said second processor core;~~, said method further comprising:~~

detecting an event associated with said processor within a data processing system;

initiating a platform-independent device removal sequence for said processor in response to detecting said event associated with said processor;

saving a context of said thread in response to initiating a platform-independent device removal sequence for said processor~~device~~;

virtually ejecting said processor from said data processing system in response to initiating said platform-independent device removal sequence for said processor; and

servicing said event associated with said processor in response to virtually ejecting said processor from said data processing system.

16. (Original) The machine-accessible medium of claim 13, said method further comprising disabling said functional redundancy check mode in response to detecting said error within said at least one of said first processor core and said second processor core.

17. (Currently Amended) The machine-accessible medium of claim 16, wherein servicing said event associated with said processor ~~device~~ in response to virtually ejecting said processor ~~device~~ from said data processing system comprises:

resetting said processor; and

re-enabling said functional redundancy check mode in response to resetting said processor.

18. (Cancelled).

19. (Currently Amended) The data processing system of claim ~~18~~24, wherein said firmware interface to initiate saida platform-independent device removal sequence for said processor in response to a detection of an event associated with said processor comprises a firmware interface to generate a system control interrupt.

20. (Currently Amended) The data processing system of claim 19, wherein said firmware interface to generate saida system control interrupt comprises a firmware interface to generate a system control interrupt utilizing an INT_OUT command.

21. (Cancelled).

22. (Currently Amended) The data processing system of claim ~~21~~24, wherein said firmware interface to initiate saida platform-independent device removal sequence for said processor in response to a detection of ~~an~~ said event ~~associated with said processor~~ comprises a firmware interface to initiate a platform-independent device removal sequence for said processor in response to a detection of an error within at least one of said first processor core and said second processor core.

23. (Currently Amended) The data processing system of claim ~~21~~24, said memory further including an operating system to disable interrupts to said processor in response to an initiation of a platform-independent device removal sequence for said processor.

24. (Currently Amended) A ~~The~~ data processing system ~~of claim 21,~~ ~~wherein~~comprising:

a processor including a first processor core and a second processor core, a memory coupled to said processor, said memory including a firmware interface to initiate a platform-independent device removal sequence for said processor in response to a detection of an event associated with said processor, to virtually eject said processor from said data processing system in response to an initiation of said platform-independent device removal sequence, and to service said event associated with said processor in response to a virtual ejection of said processor from said data processing system;

a ~~said~~ functional redundancy check logic to operate said first processor core and said second processor core in a functional redundancy check mode comprises functional redundancy check logic to concurrently execute a thread on said first processor core and said second processor core; and

said memory further includes an operating system to save a context of said thread in response to an initiation of a platform-independent device removal sequence for said processor.

25. (Currently Amended) The data processing system of claim ~~21~~24, wherein said firmware interface further comprises a firmware interface to disable said functional redundancy check mode in response to said detection of an event associated with said processor.

26. (Currently Amended) The data processing system of claim 25, wherein said firmware interface to service said event associated with said processor in response to said ~~a~~ virtual ejection of said processor from said data processing system comprises a firmware interface to reset said processor and to re-enable said functional redundancy check mode in response to a reset of said processor.

27. (Currently Amended) The data processing system of claim ~~18~~24, wherein said firmware interface further comprises a firmware interface to initiate said~~a~~ platform-independent device insertion sequence ~~for said processor~~ in response to a servicing of said event associated with said processor and to virtually insert said processor into said data processing system in response to an initiation of said~~a~~ platform-independent device insertion sequence ~~for said processor~~.

28. (Currently Amended) An apparatus comprising:

a first firmware interface to detect an event associated with a processor within a data processing system, said processor including a first processor core and a second processor core in a functional redundancy check mode by concurrently executing a thread on said first processor core and said second processor core;

a second firmware interface to initiate a platform-independent device removal sequence for said processor in response to a detection of said event associated with said processor to save a context of said thread in response to initiation of said platform-independent device removal sequence;

a third firmware interface to virtually eject said processor from said data processing system in response to an initiation of a platform-independent device removal sequence for said processor; and

a fourth firmware interface to service said event associated with said processor in response to a virtual ejection of said processor from said data processing system.

29. (Currently Amended) The apparatus of claim 28, wherein said second firmware interface to initiate said~~a~~ platform-independent device removal sequence ~~for said processor in response to a detection of said event associated with said processor~~ comprises a firmware interface to generate a system control interrupt.

30. (Currently Amended) The apparatus of claim 28, said apparatus further comprising:

a fifth firmware interface to initiate said~~a~~ platform-independent device insertion sequence ~~for said processor~~ in response to ~~a~~ servicing of said event associated with said processor; and

a sixth firmware interface to virtually insert said processor into said data processing system in response to an initiation of said~~a~~ platform-independent device insertion sequence~~for said processor~~.